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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/145,139	08/28/98	VORBACH M	2885/14A

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MICHELLE M CARNIAUX
KENYON AND KENYON
ONE BROADWAY
NEW YORK NY 10004

EXAMINER	
VO,T	
ART UNIT	**PAPER NUMBER**
2781	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

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U.S. G.P.O. 2000 ; 465-188/25268

Office Action Summary	Application No. 09/145,139	Applicant(s) Vorbach et al.
	Examiner Tim Vo	Group Art Unit 2781

☒ Responsive to communication(s) filed on *Jun 16, 2000* .

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *5* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-18 and 22-47* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☒ Claim(s) *7-14, 17, and 43-47* is/are allowed.

☒ Claim(s) *1-6, 15, 16, 18-27, and 29-42* is/are rejected.

☒ Claim(s) *28* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

Part III DETAILED ACTION

Notice to Applicant(s)

1. This application has been examined. Claims 1-18, 22-47 are pending.

Specification

2. Applicant fails to response to the previous office action for changing a new title of the invention because it is not descriptive and applicant also fails to response to misnumbering for claim 26. Correction is required.

3. Claims 22-23 are misnumbered because claim 19 has been canceled. Correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

5. Claims 1-6, 15-16, 18-27, and 29-42 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Trimberger patent number 5,892,961 in view of "The Programmable Logic Data Book" by Xilinx 1994.

As for claim 1, Trimberger teaches an internal bus system for a unit (see fig 2 element 12 and col 2 lines 65-67 of the specification), comprising:

a plurality of nodes separating, a gate, a switching element, a driver and a register (see fig 2 element 12 and col 1 lines 46-53 of the specification);

a respective routing table storing setup information for connecting with the unit (see col 1 lines 46-49 of the specification);

a respective monitoring unit independently verifying whether connection can be set up within the unit (see col 1 lines 53-63 of the specification) **except** Trimberger does not expressly teaches a plurality of electrically independent bus segments provided within the unit. However, in the specification, Trimberger refers "The Programmable Logic Data Book", copyright 1994 by Xilinx, Inc. On pages 2-105 to 2-132 the book disclosed an FPGA having a plurality of buses interconnected within the memory cells (see fig 16 of the Programmable Logic Data Book). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of "The Programmable Logic Data Book" into the teachings of Trimberger because the "The Programmable Logic Data Book" provides the Trimberger's system variety of FPGA models to choose from for designing purposes such as high performance, flexibility, unlimited programming, and reliability (see page 2-105 of The Programmable Logic Data Book".

As for claims 2 and 22-23, they are rejected as applied above in rejecting claim 1. Furthermore, Trimberger teaches wherein the unit, the unit having a multi-dimensional cell architecture (see fig 2 element 12 of the specification).

As for claim 3, it rejected as applied above in rejecting claim 1. Furthermore, Trimberger teaches wherein the unit includes plurality of CPUs in a multi-dimensional arrangement (see fig 2 elements CLBs and col 3 lines 27-30 of the specification).

As for claim 4, it rejected as applied above in rejecting claim 1. Furthermore, Trimberger teaches plurality of arithmetic logic units in a multi-dimensional arrangement (see fig 5 elements 104-105 and col 7 line 12 of the specification).

As for claim 5, it rejected as applied above in rejecting claim 1. Furthermore, Trimberger teaches wherein the unit having the multi-dimensional programmable cell architecture includes at least one of a field programmable gate array and dynamically configurable gate array (see col 1 lines 22-55 of the specification).

As for claim 6, it rejected as applied above in rejecting claim 1. Furthermore, Trimberger teaches wherein the unit having the multi-dimensional cell architecture has a two dimensional programmable cell architecture (see col 1 lines 39-41 of the specification).

As for claim 15-16, they are rejected as applied above in rejecting claim 1. Furthermore, Trimberger teaches a program loading unit (see col 1 lines 39-40 of the specification), and wherein the program loading unit performs at least one of a configuration and a reconfiguration for each one of the plurality of nodes and the respective routing table of each one of the plurality of nodes (see col 1 lines 39-55 of the specification).

As for claim 18, Trimberger teaches a method for transmitting data within module, the method comprising step of:

transmitting the data between cells of a module having multidimensional cell architecture with synchronization via a plurality of bus segments (see fig 3 and col 5 lines 3-14 of the specification) **except** Trimberger does not expressly teaches a plurality of electrically independent bus segments provided within the unit. However, in the specification, Trimberger refers "The Programmable Logic Data Book", copyright 1994 by Xilinx, Inc. On pages 2-105 to 2-132 the book disclosed an FPGA having a plurality of buses interconnected within the memory cells (see fig 16 of the Programmable Logic Data Book). Therefore, it would have been obvious

to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of "The Programmable Logic Data Book" into the teachings of Trimberger because the "The Programmable Logic Data Book" provides the Trimberger's system variety of FPGA models to choose from for designing purposes such as high performance, flexibility, unlimited programming, and reliability (see page 2-105 of The Programmable Logic Data Book".

As for claim 24, it is rejected as applied above in rejecting claim 18. Furthermore, Trimberger teaches wherein the plurality of bus segments are permanently connected to a continuous bus system without delays (see fig 1 and col 16-20 of the specification).

As for claims 25 and 27, they are rejected as applied above in rejecting claim 18. Furthermore, Trimberger teaches wherein the plurality of bus segments are switched by a plurality of registers (see fig 4 elements 101, 121, 141 and col 5 line 63 to col 6 line 28 of the specification).

As for claim 29, it is rejected as applied above in rejecting claim 18. Furthermore, Trimberger teaches entering at least one of a unique determinable relative address and a unique absolute address of a target (see col 5 lines 22-31 of the specification); and

setting up the plurality of bus segments as function of the unique determinable relative address and the unique absolute address (see col 1 lines 46-48 of the specification).

As for claims 30-33, they are rejected as applied above in rejecting claim 18. Furthermore, Trimberger teaches setting up the plurality of bus segments in a first direction (see col 8 lines 40-45 of the specification).

As for claim 34, it is rejected as applied above in rejecting claim 18. Furthermore, Trimberger teaches setting up the plurality of bus segments as a function or at least one of a plurality of lookup tables and an at least one of a unique determinable relative address and a unique absolute address of a target (see col 1 lines 46-55 of the specification).

As for claims 35-36, they are rejected as applied above in rejecting claim 18. Furthermore, Trimberger teaches setting up the plurality of bus segments via a plurality of requests to plurality of nodes (see col 3 line 45 to col 4 line 4 of the specification).

As for claims 37-40, they are rejected as applied above in rejecting claim 18. Furthermore, Trimberger teaches providing data to the plurality of nodes (see col 3 lines 45-48 of the specification).

As for claims 41-42, they are rejected as applied above in rejecting claim 18. Furthermore, Trimberger teaches establishing connection via at least one node of a plurality of nodes (see col 1 45-55 of the specification).

Allowable Subject Matter

6. Claims 7-14, 17 and 43-47 are allowable over the prior of records.

7. Claims 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Tim Vo, whose telephone number is (703) 308-5862. The examiner can normally be reached on Monday-Friday from 7:00AM- 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Ayaz Sheikh*, can be reached on *(703) 305-9648 or via e-mail addressed to [ayaz.sheikh@uspto.gov]*. The fax number for this Group is (703) 308-5358.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [tim.vo@uspto.gov].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Tim Vo
Aug 9, 2000

AYAZ R. SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2700